Ada 2005 ... ECLIPSE ... RAID ... RapidIO ... CONFIGURABLE PROCESSORS

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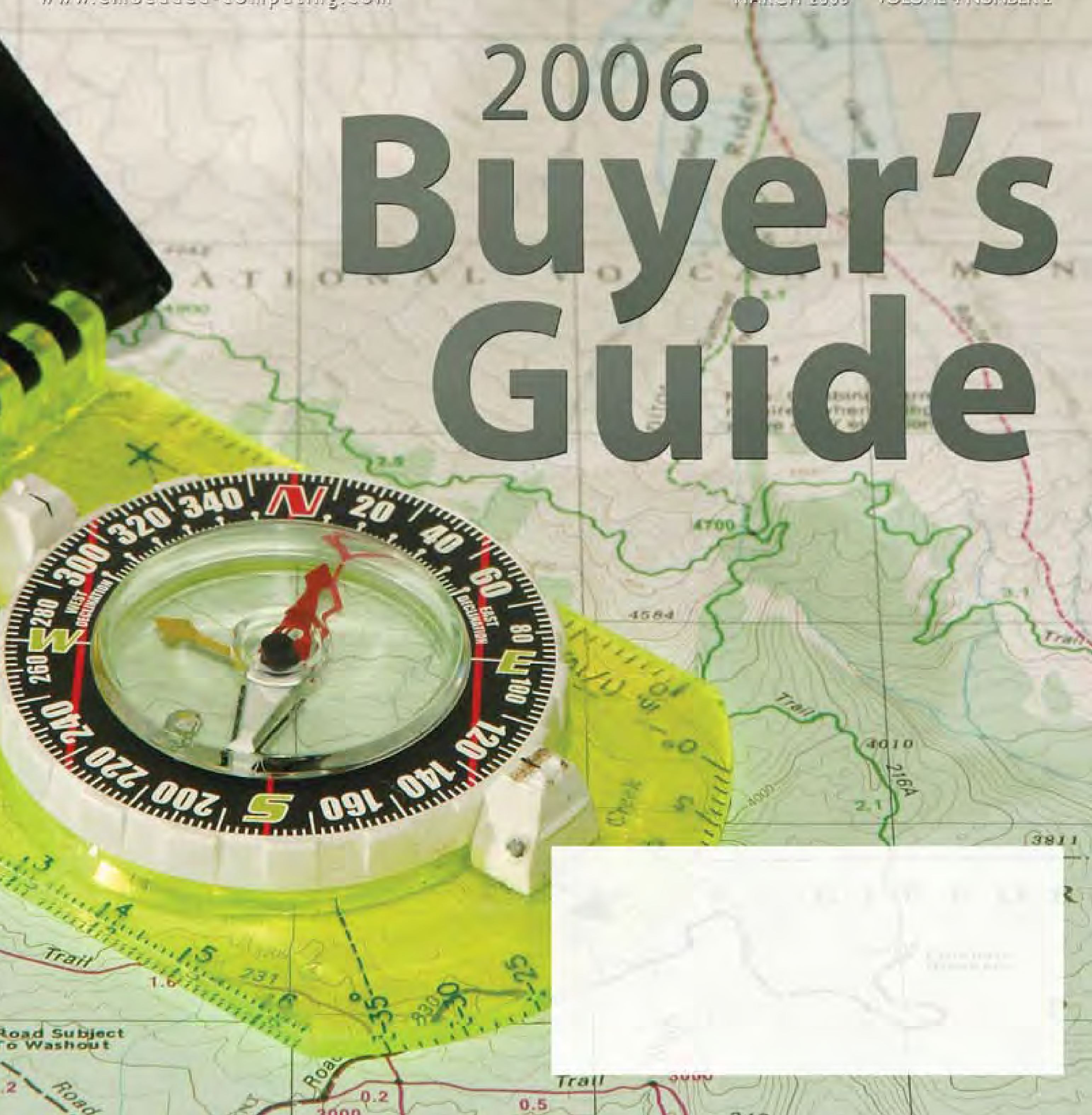
2006 Buyer's Guide



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Further defining embedded computing

Jerry Gipper

I recently attended the Consumer Electronics Show (CES) in Las Vegas. More than 1.6 million square feet of exhibits displayed the latest in consumer electronics and accessories. CES focuses primarily on entertainment devices, which fall within the scope of embedded computing. They are special-purpose computers completely encapsulated by the device they control, and for the most part perform specific predefined tasks. Products on the show floor included digital cameras, multimedia centers, wireless networks, media players, cell phones, and much more, all of which are embedded computing systems.

It continues to amaze me how much embedded electronics have changed our lives. It is virtually impossible for anyone to go through a day without being affected by many such computer systems. With the forecast indicating the impact of embedded technology on our lives will increase by orders of magnitude in coming years, *Embedded Computing Design* examines the technology, tools, and components that make embedded computing possible.

Looking deeper into the definition of embedded computing, I struggle with how to classify some types of devices. A general-purpose personal computer sitting at someone's desk, loaded with your typical office productivity suite may not be considered an embedded computer under commonly embraced definitions. A computer programmed to perform its dedicated task day-in and day-out is easy to classify as an embedded computer. But, many devices don't lend themselves to such straightforward classification. The emerging multimedia centers, for example, usually include a repackaged desktop PC with a modified user interface dedicated to managing media within a home environment, though on some models you can still do your e-mail and use a word processor.

What is a desktop PC dedicated to controlling a factory process, or a server that can be reconfigured to handle different tasks? And what is my Treo? It is more that a dedicated phone; I can download software and do word processing, presentations, take pictures, surf the Internet, and much more. The newest models even run the Windows Mobile operating system. So are these embedded computers?

I propose creating levels of classification for embedded computing. Staying within the scope of common computing terminology, I suggest we establish a range of embedded computing from Hard (or Deeply) embedded to Soft embedded with a Firm embedded in the middle. We could then place devices in the appropriate category as determined by functionality.

Why does this grey area exist? Today, many devices are connected to the Internet, allowing them to be reconfigured as needed. This makes it easier for them to be used as general-purpose computers, or reconfigured easily through interfaces like USB and removable flash devices of many types.

Table 1 gives some ideas of what I mean by my definition.

Hard embedded	Firm embedded	Soft embedded
Engine control	Smart phones	Dedicated PC
Robotics	PDAs	Multimedia centers

Table 1

Why is this segmented definition necessary? It probably has no useful technical or marketing application, but I may sleep better at night! I plan to use my definition in future issues to steer you to products and technologies appropriate for your applications. This definition is subject to change, and I will improve upon it as time progresses.

The March issue of *Embedded Computing Design* is our annual Buyer's Guide. We provide you, the designers of embedded computing systems, some useful tables to assist you in finding sources of embedded computing components of all types.

In this issue:

- *Leveraging legacy interconnect with fabric technology*, authored by Tom Cox, executive director of the RapidIO Trade Association. Tom shares how RapidIO and PCI Express technologies will likely coexist in many embedded applications. The best choice may often be to use an appropriate combination of both fabrics.
- *Extending software-configurable processors through multiple configurations*, composed by Joe Hanson of Stretch Inc. General-purpose and digital signal processors using fixed instruction sets are failing to meet compute requirements of many of today's complex embedded systems. Joe explains how software-configurable processors can be used to solve this problem.
- *Ada 2005 for deeply embedded systems*, written by Jose Ruiz, senior software engineer at AdaCore. For more than 20 years Ada has been used successfully to build embedded real-time systems with demanding requirements for reliability, safety, and performance. Ada has continued to evolve, and has become a contender as the language of choice in demanding applications.
- *Microprocessors with built-in RAID functionality: Helping streamline embedded designs*, penned by John Fakiris and Haluk Aytac of AMCC Integrated Communications Products. RAID is a widely used technique for achieving higher levels of performance and reliability from storage systems. John and Haluk tell us how microprocessors with built-in RAID functionality can streamline embedded designs and overcome the inherent limitations of software-intensive RAID solutions.

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We will continue to cover technologies of all types that shape your embedded computing designs, plus explore software and customization in embedded computing in more detail. We are always looking for interesting application stories that show how embedded computing is changing our lives and ways of doing things.

Your suggestions and comments are welcome. Please contact me at jerry.gipper@opensystems-publishing.com.

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EMBEDDED PERSPECTIVE

By Don Dingee

Bigger places for our stuff

In 1981, I was a college kid working on test equipment driven by an HP minicomputer with an HP 7905A drive unit, which contained a 10 MB removable platter drive along with a fixed 5 MB hard drive. The platter (maybe 18 inches in diameter) could be removed and locked in a cabinet to meet data security requirements. We thought 10 MB was a lot of space for our *stuff*.

Now, some mornings greet me with 10 MB of new stuff in my e-mail inbox. And four shots on my Canon Digital Rebel easily exceed 10 MB. George Carlin once said, “That’s all you need in life, a little place for your stuff.” The places we need for our stuff today have gotten much bigger, and flash memory and hard drive technology are keeping a rapid pace.

Flash gets bigger, smarter

The *New York Times* recently reported the worldwide flash market in gigabits grew 240 percent in 2005. Driven by the Apple iPod nano, video-enabled mobile phones, GPS devices, digital cameras, and other consumer electronics, flash has displaced many low-end hard drives.

Today, 8 GB CompactFlash cards are beginning to ship in volume, with hints of 16 GB out there. And the capacity is doubling every 18 months. Flash offers size, mechanical durability, and power consumption advantages difficult to match with a hard drive in small applications.

> “Driven by the Apple iPod nano, video-enabled mobile phones, ... and other consumer electronics, flash has displaced many low-end hard drives.”

Flash is also getting smarter. Gone are the concerns of short life cycles and wear out. New technology such as SiSMART from Silicon Systems is taking flash capability to new levels, with 2M write/erase cycle performance and reliability monitoring functions similar to those of enterprise-class hard drives.

If the wear algorithms work efficiently, blocks wear equally over time, said Gary Drossel, director of product marketing at Silicon Systems. So when blocks wear out and spare blocks start to be used, all the blocks are very close to being worn out.

SiSMART monitors the number of write/erase cycles applied to each flash block, and provides tracking data back to the host that gives an accurate *fuel gauge* of the remaining usable life. Instead of simply letting the flash fail suddenly and unpredictably, SiSMART helps users to model usage, set thresholds to take maintenance action, and adjust data collection to better match the life of the deployed system.

Hard drives go perpendicular

Hard drives have two distinct segments today: the microdrive and the large capacity drive.

- Microdrives are found in portable video-playback devices and a new class of mobile phones. According to IDC, this consumer electronics hard drive segment is growing at 37 percent through 2009. Today these drives are reaching 8 GB, at one-fifth of the cost of flash at the same capacity.

- Large capacity drives are winning in popular Digital Video Recorders (DVRs), home media servers, and multimedia desktop and notebook PCs. The 3.5-inch drive now ships in 500 GB.

Both these are now shipping with the latest in hard drive technology – Perpendicular Magnetic Recording (PMR), where the magnetic charge is driven deeper into the media surface instead of spread longitudinally, allowing increased density.

With a demonstrated 230 Gb/in^2 area density, and estimates of 4-5x density improvement at maturity over today’s best longitudinal technology, PMR is powering hard drive capacity. By 2007, vendors are targeting a 20 GB 1-inch microdrive, and a 1 TB 3.5-inch large capacity drive.

Cornice’s Dragon Series microdrive announced at this year’s CES packs 8 GB into a 40 percent smaller space than previous models by reducing z-height, and their Crash Guard technology features active latching, skip control, and drop safe elements to protect consumer electronics from everyday bumps and drops.

Stuff choices

Whether the choice is flash or hard drive, both technologies are thriving, and vendors are creating innovative solutions. In large capacities, hard drives still rule and are being rejuvenated with PMR. For embedded systems, flash is making huge strides, and there is some overlap between flash and microdrives; the decision comes down to use, capacity, space, power, and cost.

Designers have a range of options to store more stuff than ever before. While you think about all the stuff you have, how you’ll get more stuff, and how you’re going to store it, you can write down your thoughts on embedded computing technology and give me more stuff you’d like to hear about at ddingee@opensystems-publishing.com.

Embedded medical and space systems

By Hermann Strass

Research

Computer Tomography (CT) systems are normally used to scan living human bodies. The Supreme Council of Antiquities of Egypt uses a CT system from Siemens Medical Solutions (Germany) to scan mummies in Egypt. The mummy of Pharaoh Tutankhamun was the first to be scanned more than 3,000 years after it was embalmed. The CT system took more than 1,700 images on a truck in front of his burial chamber. AEMtec (Germany) made the photodiode array, a key element of the CT. It uses photo ASICs with 1,200 bonds on an extremely large ASIC of 2,000 mm^2 (3.1 in^2).

Magnetic Resonance Tomography (MRT), another human body-scanning technique, can scan bodies up to 205 cm (80 inches) long in one single scan in only 12 minutes (vs. 60 minutes for previous technologies). This is accomplished by using Parallel Acquisition Techniques (PATs) for image capture. Figure 1, courtesy of medizin.de, shows part of world-record swimmer Hannah Stockbauer's body scanned in a single scan. The MRT software was developed with WindRiver's VxWorks Edition development package.

Figure 1

While CTs use x-rays, MRTs use physical resonance to scan the body. CTs are better in detecting bones; MRTs are better in detecting the soft parts of a body, as demonstrated in Figure 2, courtesy of medizin.de, which portrays a human head in 3D using MRT with no radiation exposure to the patient. The *Magnetom Avanto* MRT from Siemens Medical Systems (Germany) is based on Total Imaging Matrix (TIM) technology, a matrix coil concept.

Figure 2

Standardization

Kontron (Germany) has opened the JFLEX specification for unrestricted public use. This is a mezzanine standard for JREX boards that avoids internal cables and uses Surface Mount Technology (SMT) and press-fitting on the boards (approximately 8.9 cm or 3.5-inch form factor). At first, 19 companies from Europe, the United States, and Canada supported this initiative. European patent number 01127562.5 defines a cable-free expansion module system, which can communicate with a host CPU with the PCI bus or via a Low Pin Count (LPC) bus.

Business

Congatec (Germany), a newcomer in the embedded marketplace, offers boards based on the XTX Computer-on-Module standard, which itself is based on ETX. XTX replaces the ISA bus with PCI, PCI Express, and other new I/O interfaces like SATA and USB. I2C and LPC busses are also in the standard. Congatec also offers ETX-based products.

Sensor-based measuring technology evolved about 50 years ago in Central Europe. Initially, mechanical measurement systems were equipped with an electrical signal transducer. Today, sensors play a large role in any automation system. Switching sensors have become a second pillar of European measurement

technology. Semiconductor-based piezoresistive elements now are used for about 70 percent of pressure measurement tasks. In Europe, alliances between sensor and system producers are key for getting a large share of approximately 40 percent of the world market. Sensor business in Europe is about € 15 billion per year (approximately U.S. $18 billion). Some applications are way out … on Mars. About 70 Magneto-Resistive (MR) sensors manufactured in Germany control NASA’s OPPORTUNITY and SPIRIT on Mars.

> “Switching sensors have become a second pillar of European measurement technology.

LMS International (Belgium) provides solutions for functional performance engineering in product development designs based on dynamic behavior such as motion, ride, handling, vibration, acoustic, NVH, and fatigue lifetime. LMS also provides vehicle development support from overload contracting and troubleshooting, technology transfer, up to codevelopment projects. Caterpillar uses solutions from LMS to optimize vibration effects and reduce noise in their products. Aisin Seiki, a Japanese supplier of automotive products, uses LMS Virtual Lab Motion simulation software to improve the dynamic performance of vehicle components like electronically controlled door opening systems, Retractable Hard Tops (RHTs), or seat adjustment. General Motors uses test systems from LMS for noise reduction design. The LMS system supports the updated ISO 362 standard for measurement of noise emitted by accelerating road vehicles.

Future development

Deeply embedded computer systems operate a subway train in Nuernberg (Germany). This train, which has no driver, is currently being tested within the subway system of Nuernberg. Public service is planned to start sometime in 2006. Other innovative embedded systems integrated into this driverless train include door sensors that see and feel obstacles and a control center that passengers can communicate with in case of emergency.

MPL AG (Switzerland) has developed the MIP405 computer system in embedded space applications. The MIP405 is equipped with the highly integrated embedded PPC405GP PowerPC processor from IBM. After testing, NASA found it to be immune against ion and proton radiation up to 200 MeV. NASA did not find any *destructive latch-ups* or *single event burnouts*, and plans to use the MIP405 in space shuttles and the International Space Station (ISS).

Events

The SENSOR + TEST 2006 International Trade Fair for Sensorics, Measuring, and Testing Technologies is held from May 30-June 1 in Nuernberg. The showcase for the world’s test and measurement community, SENSOR + TEST 2006 is colocated with MeasComp, a focused forum for measuring technology specialists. Dates for fairs and other events had to be rescheduled because of the world soccer championship in Germany this year. Be sure to put this on your calendar if you are in the sensor or test and measurement industry.

Five win-win advantages to truly open source plug-ins

By Michael McCullough

As there are now many vendors creating and delivering plug-ins for the Eclipse framework, it makes sense to explore some of the advantages of plug-ins supplied as completely open source code. Completely or truly open source code means that not only does the user get the source for the plug-in, but they also get all the associated files necessary to rebuild the product themselves. Many vendors currently deliver plug-ins as prebuilt Eclipse executables without any source code whatsoever. While this may be how IDE products were delivered in the past, these vendors are missing out on many of the advantages that open source really provides.

If leveraged properly, vendors creating truly open source plug-ins can translate these advantages into better user satisfaction, and can help resolve other issues implicit in the user's choice of Eclipse as a development framework.

1) If it's free, it's for me

Users win: Code transparency. Many software developers familiar with open source immediately understand the benefit of being able to see the code. Developers view access to the source code as added insurance – not only to better understand the original developers' intent, but for dealing with potential problems down the road as well. The ability to "just read the code" and possibly devise alternatives to change or correct its behavior is powerful.

Vendors win: Reduced product support. In most cases having the source code available actually decreases the amount of experienced product support personnel and time needed to deal with user questions, effectively lowering the overall cost of product maintenance to the vendor.

2) It's a stretch, but …

Users win: Extending functionality. Sophisticated users may decide to add their own new functionality to the plug-in. By customizing the product to their needs, users can reduce the need to relearn different interfaces in future revisions.

Vendors win: Enhanced products. Smart vendors can make appropriate arrangements with their users to incorporate the new functionality into later revisions of the product. This builds a motivated, loyal user community, while at the same time reducing product development costs.

3) Getting experienced

Users win: Better services. What if the vendor provides the source code and a buildable project, and users are *still* not comfortable changing the product without additional support? In these cases, many vendors provide extended product (and Eclipse) training or consulting and respond quickly to their users' needs.

Vendors win: Increased value. Vendors committed to professional services can become more of a valued partner to their users, and may even be asked to take on more responsibility for the overall success of the entire environment.

4) Merging traffic

Users win: Better integration. Many vendors provide a complete Eclipse directory tree with their own proprietary plug-ins already embedded in it. This is done to ensure that the user has a complete, working, tested Eclipse environment to work under. But, what if the user is working with two different products from different vendors who both distribute Eclipse directories with their products? In many cases it may be difficult or even impossible to effectively create a merged Eclipse solution. The user can rebuild the original plug-in and complete the integration of the two products into a single unified whole – with or without vendor assistance.

> "The ability to "just read the code" and possibly devise alternatives to change or correct its behavior is powerful.

Vendors win: More integration opportunity. The clever vendor can now become more of an Eclipse integrator for their customer than simply the vendor of a single aspect of the environment. Vendors must understand that this problem is not uncommon and know how to react appropriately, and they may need to commit themselves to a more total *development environment as a whole* concept than they have in the past. For instance, vendors may require consulting support to better deal with the external products they may face.

5) Go, team, go!

Users win: Less risk. Finding a solid, cooperative vendor producing a quality product reduces risk in using their product and services. This shared risk helps the user focus on their specific value-add tasks during their development effort.

Vendors win: Happy users. If the vendor can effectively assist the customer through additional training or consulting services work, the user will probably view the vendor as more of a willing and able partner in their own work. At the very least, users will perceive the vendor as actually concerned with helping them achieve success in their development.

Everyone wins with truly open

By viewing the source code as part of the product and creating well-written and maintainable code, vendors can catalyze the benefits for both themselves and their users. When the source code is as easy to use as the product, then users will develop a healthy respect not only for the deliverable product (and vendor), but also for the engineers who developed it.

With truly open source plug-ins done right, both users and vendors win. They now can leverage the best capabilities of the open Eclipse environment to build better business relationships for both parties. And don't all users want to have a more productive relationship with their vendors?

Michael McCullough *is president and CEO of MCC Systems, Inc. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. A 20-year electronics veteran, he has held various positions at Wind River Systems, Lockheed Sanders, Stratus Computer, and Apollo Computer. MCC Systems is a provider of Eclipse-based software development tools, training, and consulting services for the embedded systems market.*

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SIDEBAR

Eclipse News

Lattix launches LDM, joins Eclipse Foundation

Lattix Inc. (Andover, MA) has developed a new lightweight approach that utilizes system interdependencies to create an accurate blueprint of large, mission-critical software systems. Lattix LDM uses Lightweight Dependency Models, a dependency structure matrix for a highly compact and scalable representation of an entire system, providing high-level visibility for the entire development organization. Lattix LDM also incorporates design rules to allow the formalization and automated enforcement of subsystem interdependencies, including external libraries.

Lattix LDM for Eclipse provides these unique capabilities:

- Map architecture to actual code, including examining subsystem code with its associated dependencies
- Test architecture and detect architectural violations while coding
- Combine architectural remediation suggested by Lattix LDM with Eclipse refactoring capabilities in order to decouple subsystems, remove unwanted dependencies, and rename subsystems so that the code organization reflects the intended architecture

Lattix has also joined the Eclipse Foundation as an Add-In Provider member. "Our customers are very excited about having the capability in Eclipse to map their application architecture to the actual code," said Neeraj Sangal, president and founder of Lattix. "They now will have the means to test the architecture, detect violations while coding, and prevent architectural erosion."

For more information, see www.lattix.com.

Objectives for CDT project

At the October 2005 C/C++ Development Tools (CDT) Contributors Summit, more than 20 companies participated in setting the near term course for the CDT project.

At this summit, priorities for the next release of the CDT code base were established, including:

- Improved build management and debugging
- A new indexer, called the Persisted Document Object Model (PDOM), aimed to improve system performance
- Easing the commercial build process on the CDT framework through finer-grained componentization and more concise API documentation

Representatives from the Tools Platform Device project, Device Software Development Platform (DSDP) project, and Photran and Parallel Tools projects were also present, discussing easier third-party integration and tool migration between projects.

"The CDT project is maturing, and the participation of such a wide cross-section of companies at the conference is a testament to the importance CDT plays in development systems for vendors and users of tools alike," said Doug Schaefer of QNX Software Systems, project leader for the CDT.

Participating companies included Altera, Cisco, ENEA, Ericsson, Etnua, Freescale, IBM, Innoopract, Intel, Los Alamos, Mentor Graphics, Montavista, Nokia, QNX Software Systems, Siemens, Symbian, Texas Instruments, Tensilica, UIUC, and Wind River.

For more information, see www.eclipse.org/cdt.

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Continued on page 18

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Continued on page 20

COMMUNICATIONS

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Leveraging legacy interconnect with fabric technology

By Tom Cox

Today, many designers and engineers working with next generation embedded systems believe they need to choose between PCI Express and Serial RapidIO and the unique benefits each brings to the market. In reality, these two interconnects often work extremely well in tandem in a wide range of embedded applications and deliver the high performance needed by today's evolving market. This article will provide a high-level perspective and introduction to how these interconnects work together to maximize performance and lower costs.

Best available solutions

Today's embedded applications space is as diverse as any engineering design challenge can be, and continues to grow in complexity. Standards and specifications for reliability, scalability, performance, and cost are unique to every design. Despite marketing claims, there never has been a single perfect solution to these challenges, nor will there ever be one. As such, identifying and selecting the best available solutions to solve real-world application challenges remain fundamental principles in embedded computing design.

System I/O and legacy interfaces have always been an important part of embedded design. System I/O devices including hard drives, networks, and real-time data and proprietary interfaces are found in a many systems. Likewise, legacy interfaces like PCI have been part of embedded computing applications since PCI revolutionized the PC Enterprise space more than a decade ago.

Since its introduction, PCI has been used extensively in embedded applications and has evolved through several generations of speed, bus width, and protocol (PCI-X and Serial PCI Express). It is important to note that PCI in embedded designs differs greatly from the PC Enterprise application. In deeply embedded designs PCI is most often used with non-x86 processors, multiple processors, and diverse I/O devices. It is almost never used with PC architecture or standard PC BIOS, OS, and drivers. PCI and PCI Express used in embedded designs are often direct interfaces from processors and multi I/O-supported devices.

Switch fabrics using serial interconnects, by comparison, are the market revolution and the backbone in the development of new systems that require increased performance, lower cost, modularity, and reuse. New design challenges with legacy chip-to-chip interconnects that need to be supported across the backplane as a fabric can be solved by having a common protocol and physical interface while simultaneously offering advantages in the overall system architecture. The solution relates back to the basic principle of design: taking the best available solutions in serial interconnects – PCI Express and RapidIO – and using both to leverage legacy PCI within embedded switch fabric technology.

Collaborative benefits

The RapidIO standard was designed specifically as a widely applicable, flexible, extensible system fabric for embedded infrastructure equipment including networking, storage, and communication systems. Specifically, RapidIO technology

is targeted at the intrasystem interconnect applications in the high-performance embedded equipment market. PCI Express is not well suited to being a fabric, as PCI Express hubs need to fully terminate the protocol to "emulate" a switch function.

RapidIO technology bridges PCI and PCI Express more efficiently than any fabric, using low protocol overhead and direct transaction mapping. Packet overhead and data size are the answer to determining efficiency; RapidIO technology has the highest effective bandwidth using small efficient headers, an advantage in embedded systems where data payload sizes are often 256 bytes or less. RapidIO technology contains a rich set of operations and capabilities to transport PCI in a transparent manner, with one-to-one transaction maps defined in the spec. Bridges to translate PCI transactions to RapidIO transactions are simple and available today in FPGAs and Application-Specific Standard Products (ASSPs).

Efficiency is not only found in the direct mapping of PCI functions to RapidIO functions. Direct peer-to-peer communications enhance system-level performance – source directed routing, a message-passing protocol, classes of service, multicast transactions, and topological flexibility. RapidIO technology offers a full complement of flexibility, optimizing data flow and direct peer-to-peer communications with no extra overhead or latency. RapidIO technology also has a full range of flow-control mechanisms defined in its data-streaming control layer, adding congestion control and fine-grain end-to-end flow control. Moving from traditional bus technologies to switch fabrics and serial interconnects offers many choices like Star, Dual-Star, Mesh, Daisy-chain and Tree. These additional efficiencies can often provide orders of magnitude gains in performance.

Summary

Developing a solution that bridges the old with the new can be achieved with the functionality delivered with RapidIO technology and PCI/PCI Express. These interconnects are complementary technologies that leverage the I/O subsystems and the infrastructure of PCI and high-performance switched fabrics designed to address the embedded computing market's unique requirements. ECD

Tom Cox *is the executive director and a founding member of the RapidIO Trade Association. During his 26-year career, he has earned a reputation as an interconnect expert, both from a technical and market perspective based on his knowledge of systems, applications, and chips, as well as his vast experience in both industry associations and market-leading corporations.*

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Extending software-configurable processors through multiple configurations

By Joe Hanson

General-purpose and digital signal processors using fixed instruction sets are failing to meet compute requirements of today's complex embedded systems. Introducing hardware acceleration provides the necessary performance increase, but at the cost of increasing complexity and extending the overall design cycle.

Complex compute-intense functions can be converted into a single instruction through software-configurable processors, which have resources that can be extended easily under the control of the software programmer through multiple configurations. This article will describe the architecture of a software-configurable processor and the mechanisms for loading individual configuration contexts.

Software-configurable processors

Software-configurable processors integrate programmable logic as part of the processors execution pipeline, which is accessed in the same way as any functionality in the processor: via software instructions. Complex algorithms can be reduced to a handful of optimized custom instructions that each represent hundreds of lines of C code executed in a highly parallelized pipeline. Such calculations execute in tens of cycles, down from hundreds or thousands of cycles, increasing the computational capacity of the processor for this specific application. Unique software instructions loaded into the programmable logic effectively configure the processor to the software application. As the developer writes new software, custom software instructions can be created to greatly reduce the number of processor cycles required. As the software developer continues to improve the algorithm(s), the processor continues to be configured (customized) to meet the new requirements.

The S5 software-configurable processor architecture from Stretch (Figure 1) simplifies the configuration of programmable logic through a tightly integrated software development environment. The software-configurable processor architecture is the first off-the-shelf implementation of the Xtensa Instruction Set Architecture (ISA), a configurable and extensible processor developed by Tensilica. The Xtensa ISA provides the base mechanisms for supporting custom instructions implemented in hardware as part of the execution pipeline. Stretch extended the flexibility of the Xtensa ISA to a higher dynamic with the introduction of an Instruction Set Extension Fabric (ISEF) and a 128-bit Wide Register (WR) file. The ISEF provides the programmable logic resources capable of holding multiple custom instructions, and is run-time configurable and reloadable. The WR serves as an efficient data-passing unit between the Xtensa ISA, the ISEFs, and memory.

Developing applications for software-configurable architectures follows the same process as the traditional software development cycle. An integrated development environment manages the project and acts as a front end to the development tool chain, including compiler, debugger, and profiler. When it comes time

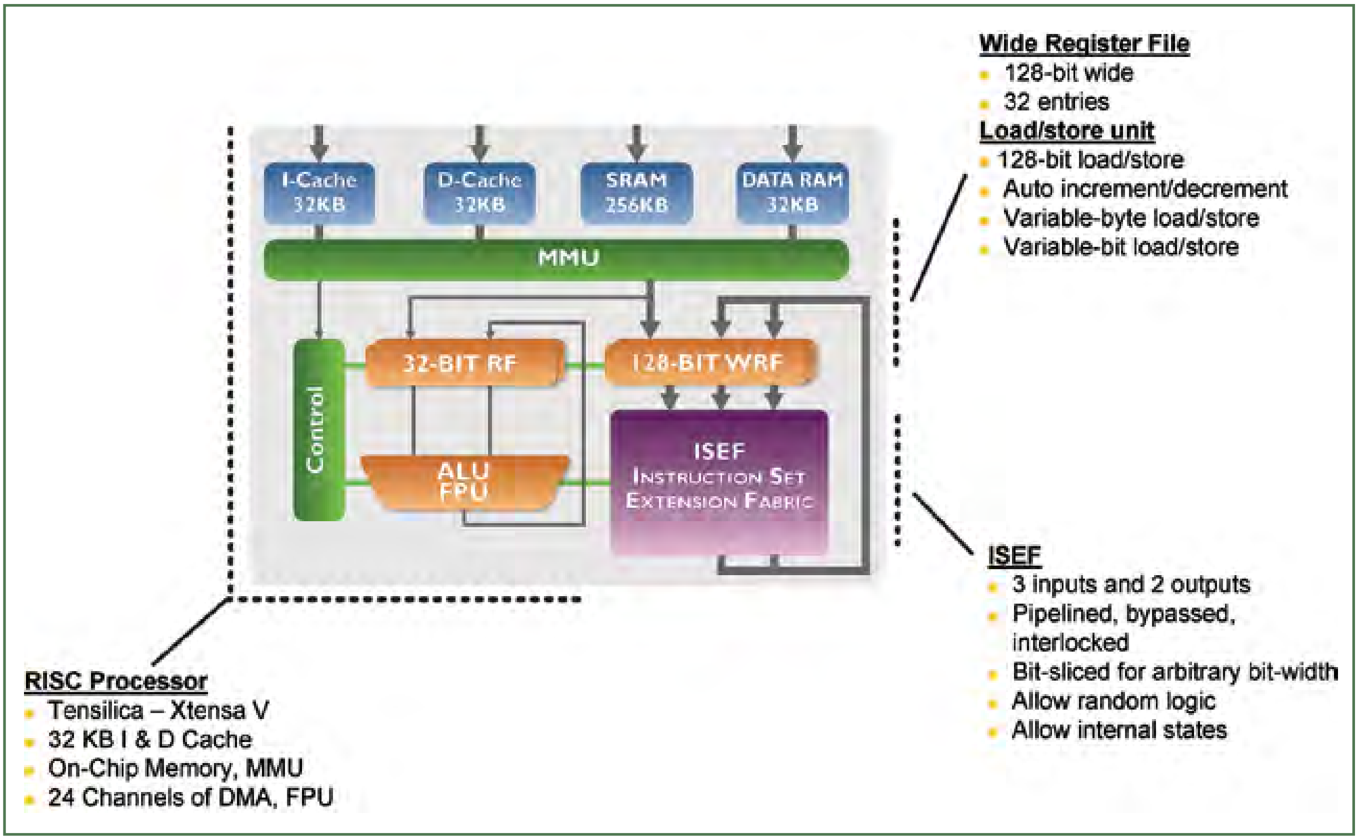


Figure 1

to improve application performance, however, rather than hand-coding assembly language or, for FPGA coprocessor architectures, passing the software algorithm to a second hardware development team to implement the function in hardware, developers instead identify "hot spots" within the program. This enables the compiler to accelerate algorithmic code by creating an extension instruction. Without requiring additional programming from the developer, the compiler creates an optimized configuration to be implemented in a programmable fabric and schedules the instruction as it would any other instruction. Developers can then profile the performance of the extension instruction. If required, the function can be characterized to process multiple data words in parallel.

Accessing this configurable functionality as software instructions has a tremendous impact on the way system developers approach embedded design. Even though the custom instructions are implemented in hardware, that is, programmable logic, developers create and use them in an entirely software context. This keeps the design of the system in a single development environment, which is both conventional and familiar to software developers. If a change in application code results in a change in the custom instructions, the compiler handles the details, rather than requiring two teams to rearchitect their hand-optimized logic based on the new partitioning.

Since both hardware and software functionality is captured in the same application code, the compiler plays an essential role in the abstraction of custom instructions and their partitioning into hardware and software resources. The Stretch C compiler manages the abstraction of custom instructions in application code, optimizes allocation of ISEF configurable resources, and tracks dependencies across the ISEF and the Xtensa processor. By leveraging key aspects, such as operator fusion and vectorization, the software developer can realize 10x-100x software performance through hardware acceleration directly from C/C++ software.

Operator fusion
Operator fusion combines multiple computation operations into a single instruction. As a result, an entire function is encapsulated as a single extension instruction. This operation in effect transforms a generic instruction set architecture into a highly specialized set of operations specific to the application. In the software-configurable processor, the resources of the ISEF limit the number of operations. The ISEF has proven to be large enough to hold multiple instructions in a single configuration. Since multiple instructions are often the desired goal for optimal software performance, operator fusion should be designed from the ground up with vectorization in mind.

Vectorization
Vectorization is a traditional stage of hardware acceleration. The ability to process multiple words of data with a single instruction (Single Instruction Multiple Data or SIMD architecture) is critical for improving performance without having to clock processors at higher frequencies, ultimately leading to greater manufacturing cost and increased power consumption.

One capability important to overall performance efficiency is the ability to work with different data sizes and data formats. Limited choice of data width and format constrains the use of fixed instructions. For example, depending upon the application and task at hand, the ideal data size may not be byte (8 bits), half-word (16 bits), or word (32 bits) oriented. The ideal size may be better specified in bits. The advantage of a software-configurable architecture is that data size and format can be determined on an instruction-by-instruction basis. It is unnecessary to convolute data to fit the size of the instruction; extension instructions can be designed specifically to match data to reduce parsing overhead, maximize resource usage, and achieve maximum performance. In doing so, multiple data objects can be passed to the extension instruction through one or more of the 128-bit WRs. Through simple extraction and concatenation operators, the Stretch C compiler arranges the data easily for the compute operations.

ISEF configuration
In some applications, a single ISEF configuration satisfies the compute requirements. However, as the compute requirements increase, so does the need for more specialized instructions. At some point the capacity of the ISEF will be exceeded and the instructions will need to be organized into different configurations. Various factors should be considered in supporting multiple ISEF configurations, including the number of extension instructions held in a single ISEF, mechanisms for loading different instructions, and how long it takes to load.

The configuration time for the S5 architecture is approximately 100 μsec (32 K processor cycles). Considering this, the decision to use multiple configurations requires that at least this many cycles will be saved. Using the software profiling tools provided in the Stretch Integrated Development Environment (IDE) determines the number of cycles consumed by the processor. These tools report the number of times the function is called and the number of cycles consumed. Once the functions are identified, the organizing into extension instructions configuration requires understanding the algorithm and the resource usage inside the ISEF.

The ISEF unit in the S5 architecture can implement 16 extension instructions in a single configuration. To the first order, ISEF

resource utilization can be estimated by looking at the number of multiplications and additions inside the function. Figure 2 shows the resource utilization by operation. The S5 ISEF contains 8 K Multiplier Units (MU) and 4 K Arithmetic Units (AU), and 4 K state registers supported by the necessary logic and routing resources. When multiplying A x B, the number of MUs required is the product of the number of bits for A and B, for example, a 16 x 16 multiplier requires 256 MUs. For addition and subtraction operations, the number of AUs consumed is the same as the size of the larger datum, for example, a 16-bit + 32-bit value requires 32 AUs. During development, resource utilization and the cycle counts are reported by the development tools.

The S5 architecture provides two independent ISEF blocks. For applications with one or two configurations, both configurations will be loaded during initialization and instructions from either ISEF can be used. For applications with two or more configurations, the BIOS will automatically manage the loading of instructions. When a user-defined instruction is issued, the S5 hardware checks to make sure the corresponding configuration is loaded into one of the two ISEFs. If the required configuration is not present in either ISEF, it is automatically loaded prior to the execution of the user-defined instruction.

The automatic system uses the simple Least Recently Used heuristic to determine which configuration to swap out in order to load a new configuration. In most applications, the developer overtaking control and loading the desired configuration in anticipation of its usage minimizes this delay. The S5 architecture supports the background loading through the use of a BIOS call. The BIOS call, sx_isef_load_by_name_async(), loads the requested configuration

C Operators	AU	MU
A*B	0	|A|*|B|
A(+,-)B	max(|A|,|B|)	0
A(<<,>>)B	0	$\|A\|*2^{\|B\|}$
A(&,^,|)B	max(|A|,|B|)	0

Figure 2

to the specified ISEF using a dedicated DMA engine. This function is nonblocking, that is, sets up the DMA and returns, and can be called again to configure the other ISEF.

While loading one of the ISEFs, the instructions in the other ISEF can continue to be used as well as the Xtensa's processor pipeline. In effect, with proper scheduling the processor will continue to operate without stalling or looping to check for status and availability.

Another key benefit of this development flow is that it keeps design in a single development environment that is well established and

> Specialized computations on specialized application data sizes and formats increase flexibility and optimize the use of computational resources.

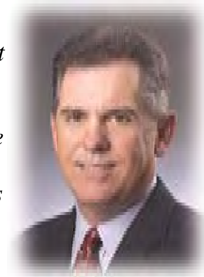
familiar to software developers. FPGA-based architectures require the use of the second development team, and any repartitioning of application code requires a rearchitecting of hand-optimized logic to match the new partitioning. With a software-configurable processor, the compiler is responsible for rearchitecting. This means that even though extension instructions are implemented in programmable hardware, developers design, create, and use them entirely in a software context.

Together, all of these factors have a tremendous impact on the way developers approach application design. A single development team can create an application, and enabling concurrent software and hardware development can significantly reduce development time without time-consuming hand optimization.

Conclusion

Through the use of software-configurable processors, developers can implement hardware acceleration for compute-intensive algorithms by means of extension instructions coded in C/C++. Extension instructions provide the performance of hardware implementations with the flexibility of software design. Specialized computations on specialized application data sizes and formats increase flexibility and optimize the use of computational resources. By describing software and hardware functionality using a single programming language and development tool chain, a development team can design hardware and software concurrently, significantly reducing time-to-market.

The flexibility of dynamically loading multiple instruction configurations into software-configurable processors also enables developers to extend the number of custom instructions available for increasing the compute performance of the processor based on the application. **ECD**



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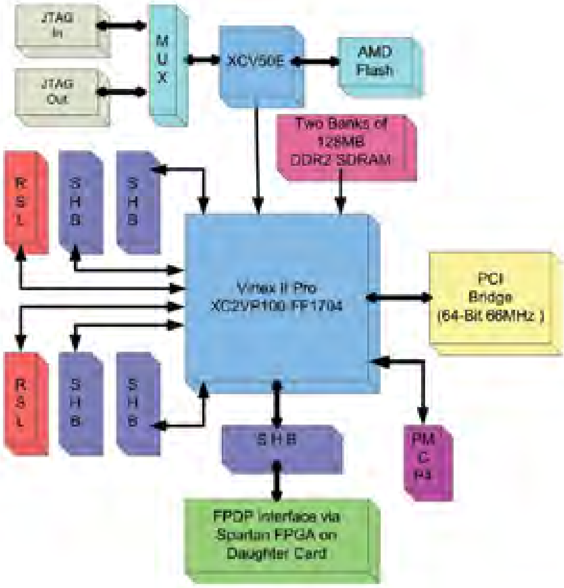

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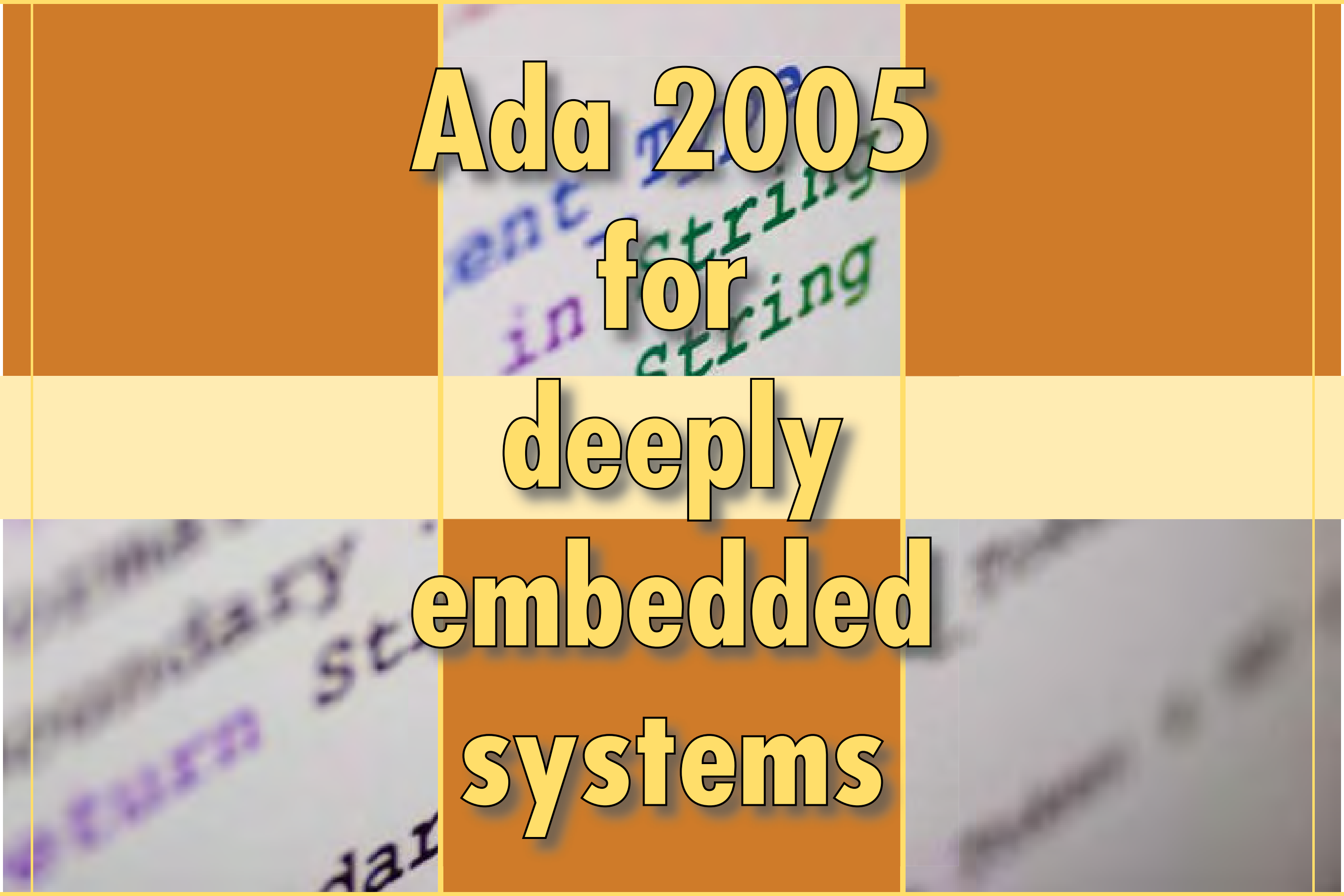

Ada 2005 for deeply embedded systems

By Jose Ruiz

For more than 20 years Ada has been used successfully to build embedded real-time systems with demanding requirements for reliability, safety, and performance. During this time the language has evolved based on user experience, and the forthcoming Ada 2005 standard includes a number of enhancements that will be of particular benefit to developers of embedded systems.

The Ada 2005 standard features support for run-time profiles, flexible task-dispatching policies, execution-time clocks and timers, and a unification of concurrency and object-oriented features. Among these new facilities, one of the most significant is the standardization of the Ravenscar tasking profile. This subset of Ada tasking features embodies a deterministic concurrency model inherently amenable to static analysis and implementable by a small, reliable, and extremely efficient run-time library. The Ravenscar profile brings modern software engineering techniques to deeply embedded systems with limited resources by providing the abstraction and expressive power that help make software easier to design and test, but without compromising performance or safety.

Ada was designed with embedded applications in mind from the start. For example, the use of representation clauses, which have been extended and made more powerful in Ada 2005, allows close mapping of data structures to the hardware (the desired location, size, alignment, and layout of data in physical memory can be specified). The use of Ada high-level constructions facilitates development, code reviews, and analysis, and Ada's strong typing allows for compile-time verification that helps early detection of errors in the development process. Additionally, many embedded applications require high reliability or are safety critical, which allows a language designed for maximum safety to really shine. More than 99 percent of the aviation software in the Boeing 777 is in Ada.

Subsetting the language

Ada 2005 may be regarded not as a single language, but rather a family of languages. In practice, when writing embedded software, one does not want to use the full facilities of a complex language since resources are scarce. Instead, software writers can choose a reduced subset that can be supported by a compact run-time system with a reduced footprint. Another advantage of this subsetting is the reduced complexity, which facilitates the generation of proofs of correctness, predictability, reliability, or coverage analysis, if needed.

The notion of Ada subsets is built into the language standard, rather than being external to it (such as the MISRA C subset). Additionally, the application developer can choose the specific features in the subset, thus providing a high degree of flexibility. Any attempt to use excluded features will be flagged as a compile-time error, and importantly, the implementation can exclude from the executable any run-time support for what is forbidden, thus reducing the memory footprint of the application.

The Ravenscar tasking profile

As the functionality and complexity of embedded software increase, more attention is being devoted to high-level, abstract development methods. The Ada tasking model provides concurrency as a means of decoupling application activities, hence making software easier to design and test.

The tasking model in Ada is extremely powerful, but it may be considered relatively complex, resource consuming, and difficult to analyze. The Ravenscar profile is a subset of Ada tasking that provides the basis for the implementation of simple, deterministic, and time-analyzable applications. This subset is amenable to static analysis for high integrity system certification, and can be supported by a small, reliable, and efficient run-time system.

The Ravenscar profile is founded on state-of-the-art, deterministic concurrency constructs adequate for constructing most types of real-time software. Major benefits of this model are:

- Improved memory and execution time efficiency by removing high overhead or complex features
- Increased reliability and predictability by removing nondeterministic and nonanalyzable features
- Reduced certification cost by removing complex features of the language, thus simplifying the generation of proof of predictability, reliability, and safety

The profile is based on a computation model, which includes the following features:

- A single processor
- A fixed number of tasks
- A single invocation event per task (either time-triggered or event-triggered tasks)
- Task interaction only by means of shared data (protected objects) with mutually exclusive access

The tasking model defined by the profile includes tasks and protected types and objects at the library level, a maximum of one protected entry with a simple Boolean barrier for synchronization, a real-time clock, absolute delays, preemptive priority scheduling with ceiling locking access to protected objects, and protected procedure interrupt handlers, as well as some other features, which allow the development of embedded real-time systems.

Constructs that are difficult to analyze, such as dynamic tasks and protected objects, task entries, dynamic priorities, select statements, asynchronous transfer of control, relative delays, or calendar clock, are forbidden. Ravenscar's simplicity allows memory usage and execution to be efficient and deterministic.

The Ravenscar tasking model is static, so the complete set of tasks and associated parameters (such as their stack sizes) are identified and defined at compile time; thus the required data structures (task descriptors and stacks) can be created statically by the compiler as global data. Therefore, memory requirements can be

determined at link time, and the use of dynamic memory can be avoided.

The Ravenscar profile, part of the Ada 2005 standard, helps achieve source code portability. The intention is that not only will Ravenscar be implemented, but in appropriate environments (notably embedded environments), efficient implementations of the Ravenscar tasking model will also be supplied.

Scheduling and dispatching policies

An important area of increased flexibility in Ada 2005 is that of task-dispatching policies. In Ada 95, the only predefined policy is fixed-priority preemptive scheduling, although other policies are permitted. Ada 2005 provides further pragmas, policies, and packages, which facilitate many different mechanisms such as nonpreemption within priorities, round robin using timeslicing, and Earliest Deadline First (EDF). Moreover, it is possible to mix different policies according to priority levels within a partition.

Execution time monitoring and control

Monitoring and controlling execution time is important for many real-time systems. Ada 2005 provides an additional timing mechanism, which allows for:

- Monitoring execution time of individual tasks
- Defining and enabling timers and establishing a handler that is called by the run-time system when the execution time of the task reaches a given value
- Defining an execution budget to be shared among several tasks, providing means whereby action can be taken when the budget expires

Monitoring CPU usage of individual tasks can be used at run time to detect an excessive consumption of computational resources, which usually are caused by either software errors or errors made in the computation of worst-case execution times.

Schedulability analysis is based on the assumption that the execution time of each task can be estimated accurately. Measurement is always difficult, because with effects like cache misses and pipelined and superscalar processor architectures, the execution time is highly unpredictable. Run-time monitoring of processor usage permits detecting and responding to wrong estimations in a controlled manner.

CPU clocks and timers are also key requirements for implementing some modern real-time scheduling policies, which must perform scheduling actions when a certain amount

"The Ada tasking model provides concurrency as a means of decoupling application activities, hence making software easier to design and test.

of execution time has been consumed. Providing common CPU budgets to groups of tasks offers the basic support for implementing aperiodic servers, such as sporadic servers and deferrable servers in fixed priority systems, or the constant bandwidth server in EDF-scheduled systems.

Timing events

Timing events allow for a handler to be executed at a future point in time in an efficient way, as it is a standalone timer that is executed directly in the context of the interrupt handler (it does not need a server task).

The use of timing events may reduce the number of tasks in a program and the overhead of context switching. It provides an effective solution for programming short time-triggered procedures and implementing some specific scheduling algorithms, such as those used for imprecise computation. Imprecise computation increases the utilization and effectiveness of real-time applications by means of structuring tasks into two phases (one mandatory and one optional). Scheduling algorithms that try to maximize the likelihood that optional parts are completed typically require changing asynchronously the priority of a task, which can be implemented elegantly and efficiently with timing events.

Object-oriented programming

Developers of embedded software often want to take advantage of the power of object-oriented programming. Given Ada's emphasis on flexibility and reliability, Ada 2005 directly addresses the use of object-oriented methods in a configurable and safe way.

Ada's type extension and inheritance are powerful and lightweight object-oriented mechanisms useful for embedded programming. Dynamic dispatching is also available, but a language-defined restriction (*No_Dispatch*) can be used for forbidding its use, allowing for more efficient and predictable execution. Ada 2005 offers very fine-grained control over inheritance by allowing each operation to declare explicitly if it is intended to inherit, and the compiler checks that the intention is met. This avoids accidentally confusing *Initialize* and *Initialise* for example, a well-known hazard in object-oriented languages.

Designers of Ada 95 made a conscious decision to not implement general multiple inheritance because they thought its complexities overwhelmed the benefits. But, more recently, the notion of interfaces

(or roles) has been developed as an effective alternative that gives the power of interfacing to multiple abstractions without the additional complexity of full multiple inheritance. Java proved the value of the interface concept, and Ada 2005 builds on this notion to create a new and powerful form of the interface abstraction, which also extends to the unique Ada notions of task and concurrent object, maintaining the important design principle that concurrency is a first-class citizen.

Ada 2005, the key to efficiency and reliability

Ada is a powerful and well-designed language, thoroughly reviewed as part of its standardization process, which allows an effective and efficient use of high-level abstract development methods in embedded environments, without compromising performance or safety.

Reliable and efficient tasking is promoted by the Ravenscar profile, which defines a deterministic and certifiable tasking subset, providing the high-level abstraction and expressive power needed for making software easy to design and test.

Ada 2005 also supports reliable and efficient object-oriented programming by providing a high level of configurability in how to use dynamic dispatching, and by smoothly combining the concurrency and object-orientation features. **ECD**

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SOFTWARE AND DEVELOPMENT

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Microprocessors with built-in RAID functionality: Helping streamline embedded designs

By John Fakiris and Haluk Aytac

In recent years, Redundant Array of Independent Disks (RAID) has evolved into a widely used technique for achieving higher levels of performance and reliability from storage systems. With the advent of Serial Attached SCSI (SAS) and lower cost, higher capacity Serial Advanced Technology Attachment (SATA) drives, plus an increasing requirement for high data integrity, the demand for high performance RAID solutions has heightened. Cost-effective implementation of RAID algorithms requires efficient integration of RAID hardware accelerators at the embedded processor level, using advanced I/O Processor (IOP) capabilities to overcome the inherent limitations of software-intensive RAID solutions.

Evolution of low-cost RAID requirements

RAID is a form of virtualization of hard drives, in which the client sees a single drive despite the multiplicity of physical drives. There are two primary reasons for using RAID: performance and reliability. By reading from multiple drives, RAID can mask the seek time delays for each physical drive. With RAID, the speed of the I/O technology and IOP efficiency, rather than the access speed of individual drives, binds the overall storage system performance. From a reliability standpoint, RAID allows data to be replicated across multiple physical drives, thereby reducing the single-point-of-failure risks associated with conventional storage.

RAID implementations started in servers, enclosures attached to servers, and large storage arrays attached to mainframes using the SCSI protocol. Because it is a shared bus technology, SCSI made RAID possible by allowing connection of multiple disk drives to a single compute node. Given the difficulty of creating a Storage Area Network (SAN) out of SCSI, first-generation RAID storage typically was behind either servers or mainframes. The Fibre Channel protocol created a network underneath SCSI, enabling the development of SANs. As SAN technology has matured, a new standard called iSCSI is also bringing block storage into TCP/IP networks, including Ethernet LANs and the Internet. The new SAS standard is supporting a SAN based on the SCSI protocol over a simpler topology than Fibre Channel. Meanwhile, the SAS standard is enabling SATA drives to work with the SAS protocol so that low cost drives can be attached to SANs.

Design approaches for embedded RAID solutions

RAID comes in various forms (RAID 1, RAID 0, RAID 5, and RAID 6). RAID 1 mirrors data on one drive on another drive.

This is the simplest form of RAID and the most costly because it takes two drives to store one drive worth of data. RAID 0 stripes data across multiple drives, which boosts performance, but doesn't provide fault tolerance. RAID 5 goes the next step by maintaining a parity byte for every group of data bytes. RAID 6 extends the parity concept. In addition to the normal parity (P), RAID 6 computes a second parity (Q), which allows data to be reconstituted even if two drives fail.

Note that there are two types of computations:

1. Creating tasks for drives from the virtual task that is targeting a single virtual drive
2. Performing the parity computations

The first computation is complex and therefore belongs in a processor; however, the second can be streamlined and thus implemented efficiently in hardware. The basic approaches to RAID implementation include:

- Software solutions
- External hardware solutions
- IOP hardware accelerated solutions

In the software solution, the processor on the motherboard performs both parsing the tasks for drives and computing the parities. This allows for the use of general-purpose hardware, but burdens the processor with a relatively high level of complex software overhead. Figure 1 shows the steps of software-based RAID 5 parity calculation. An external DMA in the I/O controller fetches the results into the hard drives. This approach, called RAID On Mother Board (ROMB), takes more processor, bus, and DRAM steps and also keeps the CPU on the motherboard busy.

In the external hardware accelerator approach, an embedded CPU performs the task-parsing calculations and hands off the parity calculations to the hardware accelerator. This approach overcomes the performance penalty, but can impose a significant cost penalty for the additional hardware.

The RAID-enabled IOP approach provides a more optimal solution. In addition to being a programming facility with one or more embedded processors, it includes acceleration hardware necessary for RAID computations. As shown in Figure 2, an IOP with integrated RAID 6 hardware-assist capabilities for computing dual parity (P + Q) can manage multiple stripes across multiple physical drives efficiently, while appearing to the host as a single unified storage system.

To complete the controller solution, one needs to attach an I/O uplink and one (or more) I/O downlink(s) to the processor's PCI Express ports. For example, AMCC's PowerPC440SPe has three PCI Express ports (one x8 and two x4) and a PCI-X port. This configuration provides flexibility for a connection to the host processor or an attachment of an Ethernet device for iSCSI uplink, SAS/SATA controllers for the downlink drives, and in some cases an interprocessor connection for redundancy between two controllers.

The IOP approach using a PowerPC440SPe offers a choice of two exclusive OR (XOR) engines for computing the RAID 5 parity and multiple Galois Field (GF)-based polynomials for performing the P and Q parity calculations for RAID 6, as well as various alternatives for balancing load and performance. The integrated

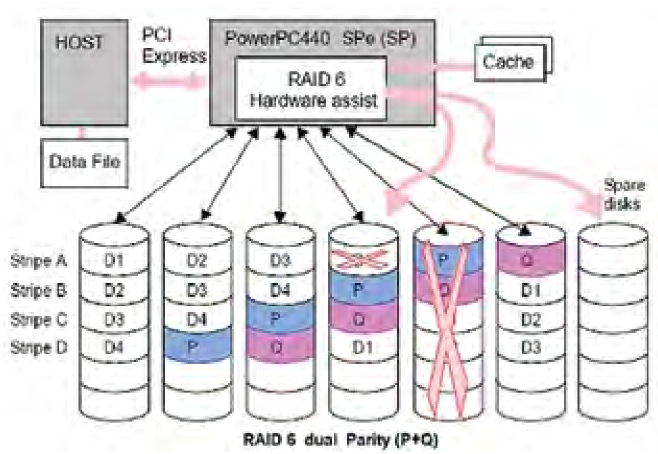

Figure 2

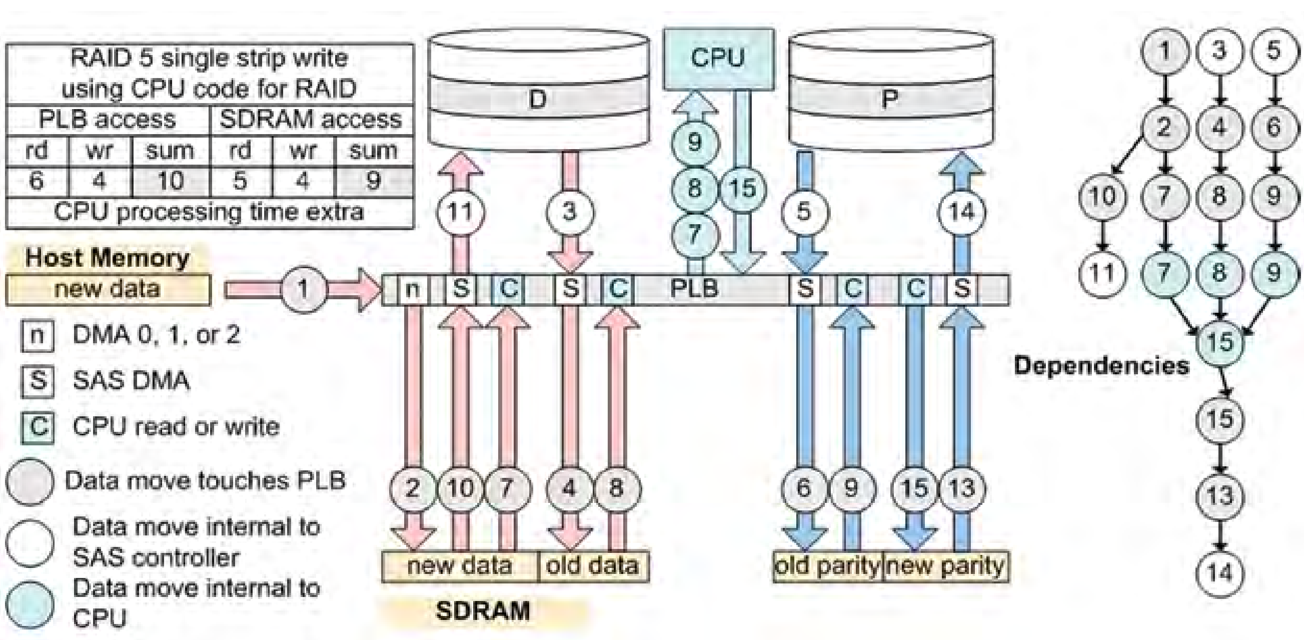

Figure 1

memory controller is dual-ported and supports up to 16 GB of 64-bit DDR667 SDRAM. To support the high-bandwidth PCI Express interfaces and memory controller, the processor local bus features a nonblocking two-way crossbar structure. The Low Latency (LL) segment implements smaller data buffers and is optimized for LL access, while the High Bandwidth (HB) segment has larger data buffers and is optimized for maximum throughput (see Figure 3).

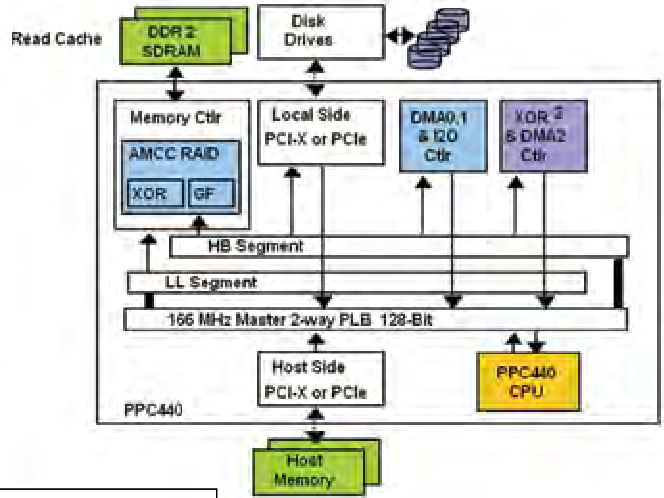

Figure 3

Summary

Demand for RAID-based reliability and performance to extend into a widening range of network-based, higher performance, and lower cost storage systems has thrust the need for embedded RAID control solutions to the forefront. Faced with these trends, designers cannot afford the performance penalty of software-based solutions or the cost penalty of external hardware accelerators. The use of highly integrated IOP devices optimized for high data throughput and RAID parity calculations and nonblocking access to standards-based I/O interfaces offers the path toward meeting stringent demands for high performance and reliability at affordable costs. **ECD**

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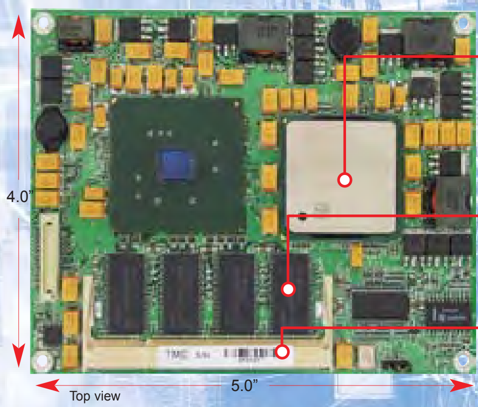

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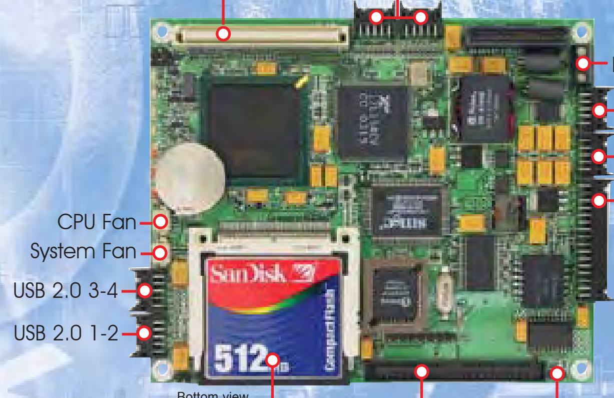

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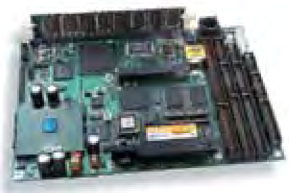

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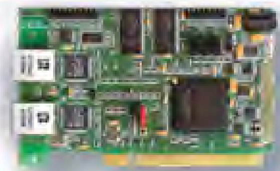

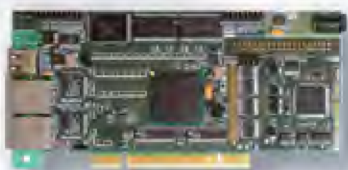

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